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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,884	08/26/2003	Chung-Che Tsai	MM4636	7826

7590 06/30/2005

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,884	TSAI, CHUNG-CHE	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *3,4,6-9,12,13 and 15-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2, 5, 10, 11 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/649884 Attorney's Docket #: MM4636
Filing Date: 8/26/2003;

Applicant: Tsai

Examiner: Alexander Williams

Applicant's election of the species III (claims 2, 5, 11 and 14), filed 4/21/05, has been acknowledged. Applicant's election was confusing since the base claim was not within the elected species. The Examiner added claims 1 and 10 to the elected.

This application contains claims 3, 4, 6-9, 12, 13 and 15-18 drawn to an invention non-elected without traverse.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence(s) of the specification or in an application data sheet by identifying the prior application by application number (37 CFR 1.78(a)(2) and (a)(5)). If the prior application is a non-provisional application, the specific reference must also include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

This application discloses and claims only subject matter disclosed in prior Application No. 10/314064, filed 12/5/2002, and names an inventor or inventors named in the prior application. Accordingly, this application may constitute a continuation or division. Should applicant desire to obtain the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120 and 37 CFR 1.78.

Claim 14 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 14, "the third chip" lacks antecedent basis.

Note: In claims 1 and 10, it is not clear if the thermal blocking member" is conductive or insulating. It appears to be insulative. T

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 and 10 are rejected under 35 U.S.C. § 102(a) as being anticipated by Tsai (U.S. Patent # 6,713,857 B1).

1. Tsai(figures 1 to 3e) specifically figure 1 show a stacked-chip semiconductor package **1**, comprising: a chip carrier **10** having an upper surface **101** and an opposite lower surface **100** and formed with an opening **102** penetrating therethrough; a thermal blocking member **13** applied at predetermined area on the upper surface of the chip carrier and over the opening, wherein the thermal blocking member has a first surface directed away from the opening and an opposite second surface facing toward the opening; a first chip **12** mounted on the first surface of the thermal blocking member and electrically connected to the upper surface of the chip carrier at area free of the thermal blocking member; a second chip **11** mounted on the second surface of the thermal blocking member and received within the opening of the chip carrier, allowing the second chip to be electrically connected to the lower surface of the chip carrier; and an encapsulant **14** for encapsulating the second chip and having a cavity for receiving and exposing the first chip.

10. Tsai(figures 1 to 3e) specifically figure 1 show a fabrication method of a stacked-chip semiconductor package **101**, comprising the steps of: preparing a chip carrier **10** having an upper surface and an opposite lower surface, the chip carrier being formed with an opening **102** penetrating therethrough; applying a thermal blocking member at predetermined area on the upper surface of the chip carrier and over the opening, wherein the thermal blocking member **13** has a first surface directed away from the opening and an opposite second surface facing toward the opening; mounting a first chip **12** on the first surface of the thermal blocking member and electrically connecting the first chip to the upper surface of the chip carrier at area free of the thermal blocking member; mounting a second chip **11** on the second surface of the thermal blocking member to be received within the opening of the chip

carrier, and electrically connecting the second chip to the lower surface of the chip carrier; and forming an encapsulant **14** for encapsulating the second chip and having a cavity **150** for receiving and exposing the first chip.

Claims 1 and 10 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sugimoto et al. (U.S. Patent # 6,874,910 B2).

1. Sugimoto et al. (figures 1(a) to 25) specifically figure 19 show a stacked-chip semiconductor package **1**, comprising: a chip carrier **4** having an upper surface and an opposite lower surface and formed with an opening penetrating therethrough; a thermal blocking member **3** applied at predetermined area on the upper surface of the chip carrier and over the opening **6**, wherein the thermal blocking member has a first surface directed away from the opening and an opposite second surface facing toward the opening; a first chip **(top 2)** mounted on the first surface of the thermal blocking member and electrically connected to the upper surface of the chip carrier at area free of the thermal blocking member; a second chip **(bottom 2)** mounted on the second surface of the thermal blocking member and received within the opening of the chip carrier, allowing the second chip to be electrically connected to the lower surface of the chip carrier; and an encapsulant **10** for encapsulating the second chip and having a cavity for receiving and exposing the first chip.

10. Sugimoto et al. (figures 1(a) to 25) specifically figure 19 show a fabrication method of a stacked-chip semiconductor package **1**, comprising the steps of: preparing a chip carrier **4** having an upper surface and an opposite lower surface, the chip carrier being formed with an opening **6** penetrating therethrough; applying a thermal blocking member at predetermined area on the upper surface of the chip carrier and over

the opening, wherein the thermal blocking member **3** has a first surface directed away from the opening and an opposite second surface facing toward the opening; mounting a first chip **(top 2)** on the first surface of the thermal blocking member and electrically connecting the first chip to the upper surface of the chip carrier at area free of the thermal blocking member; mounting a second chip **(bottom 2)** on the second surface of the thermal blocking member to be received within the opening of the chip carrier, and electrically connecting the second chip to the lower surface of the chip carrier; and forming an encapsulant **10** for encapsulating the second chip and having a cavity **5'** for receiving and exposing the first chip.

Claims 1, 2, 5, 10, 11 and 14, insofar as claims 14 can be understood, are rejected under 35 U.S.C. § 102(e) as being anticipated by Shin et al. (U.S. Patent # 6,798,049 B1).

1. Shin et al. (figures 1 to 9) specifically figure 5D show a stacked-chip semiconductor package, comprising: a chip carrier **10** having an upper surface and an opposite lower surface and formed with an opening penetrating therethrough; a thermal blocking member **34** applied at predetermined area on the upper surface of the chip carrier and over the opening **16**, wherein the thermal blocking member has a first surface directed away from the opening and an opposite second surface facing toward the opening; a first chip **1** mounted on the first surface of the thermal blocking member and electrically connected to the upper surface of the chip carrier at area free of the thermal blocking member; a second chip **2** mounted on the second surface of the thermal blocking member and received within the opening of the chip carrier, allowing the second chip to be electrically connected to the lower surface of the chip carrier; and an encapsulant **32** for encapsulating the

second chip and having a cavity **16** for receiving and exposing the first chip.

10. Shin et al. (figures 1 to 9) specifically figure 5D show a fabrication method of a stacked-chip semiconductor package, comprising the steps of: preparing a chip carrier **10** having an upper surface and an opposite lower surface, the chip carrier being formed with an opening **16** penetrating therethrough; applying a thermal blocking member **34** at predetermined area on the upper surface of the chip carrier and over the opening, wherein the thermal blocking member **34** has a first surface directed away from the opening and an opposite second surface facing toward the opening; mounting a first chip **1** on the first surface of the thermal blocking member and electrically connecting the first chip to the upper surface of the chip carrier at area free of the thermal blocking member; mounting a second chip **2** on the second surface of the thermal blocking member to be received within the opening of the chip carrier, and electrically connecting the second chip to the lower surface of the chip carrier; and forming an encapsulant **32** for encapsulating the second chip and having a cavity **16** for receiving and exposing the first chip.

In claims 2, 5, 11 and 14, Shin et al. show a third chip **3** stacked on the second chip **2** and electrically connected to the lower surface of the chip carrier **10**, allowing the third chip to be encapsulated by the encapsulant **32**; wherein the third chip **3** is electrically connected to the chip carrier **(by 20)** by a plurality of bonding wires **20**.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 11 and 14, insofar as claim 14 can be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugimoto et al. (U.S. Patent # 6,874,910 B2) in view of Huang (U.S. Patent Application Publication # 2002/0130398 A1).

Sugimoto et al. show the features of the claimed invention but fail to explicitly show further comprising: a third chip stacked on the second chip and electrically connected to the lower surface of the chip carrier, allowing the third chip to be encapsulated by the encapsulant; wherein the third chip is electrically connected to the chip carrier by a plurality of bonding wires.

Huang is cited for showing a semiconductor package which has no resinous flash formed on lead frame. Specifically, Huang (figures 1 to 8) specifically figure 6 discloses a third chip **54b** stacked on the second chip **54a** and electrically connected to the lower surface of the chip carrier **501**, allowing the third chip to be encapsulated by the encapsulant **(shown but not labeled)**; wherein the third chip is electrically connected to the chip carrier by a plurality of bonding wires **55b** for the purpose of enhancing the heat dissipating efficiency.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Huang's third chip on the second chip to modify Sugimoto et al.'s second chip structure for the purpose of enhancing the heat dissipating efficiency.

Claims 5, 11 and 14, insofar as claim 14 can be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (U.S. Patent # 6,713,857 B1) in view of Huang (U.S. Patent Application Publication # 2002/0130398 A1).

Tsai show the features of the claimed invention but fail to explicitly show further comprising: a third chip stacked on the second chip and electrically connected to the lower surface of the chip carrier, allowing the third chip to be encapsulated by the encapsulant; wherein the third chip is electrically connected to the chip carrier by a plurality of bonding wires.

Huang is cited for showing a semiconductor package which has no resinous flash formed on lead frame. Specifically, Huang (figures 1 to 8) specifically figure 6 discloses a third chip **54b** stacked on the second chip **54a** and electrically connected to the lower surface of the chip carrier **501**, allowing the third chip to be encapsulated by the encapsulant **(shown but not labeled)**; wherein the third chip is electrically connected to the chip carrier by a plurality of bonding wires **55b** for the purpose of enhancing the heat dissipating efficiency.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Huang's third chip on the second chip to modify Tsai's second chip structure for the purpose of enhancing the heat dissipating efficiency.

The following references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,784,786,678,680,774,713,712,707,717,720,783,434,782 250/239,208.1,214.1	6/25/05
Other Documentation: foreign patents and literature in 257/686,685,723,777,784,786,678,680,774,713,712,707,717,720,783,434,782 250/239,208.1,214.1	6/25/05
Electronic data base(s): U.S. Patents EAST	6/25/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/27/05